REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1, 6, 9, 11, and 15 under 35 USC § 102 (b) as being anticipated by Farrell et al. (U.S. Patent No. 5,510,740); claims 2, 3, 7, 9, and 12 under 35 USC § 103 (a) as being unpatentable over Farrell in view of Tsukikawa (U.S. Patent No. 6,121,812); claims 4, 5, 13, 14, 17, and 18 under 35 USC § 103 (a) as being unpatentable over Farrell in view of Okada (U.S. Patent No. 4,306,198); and claim 8 under 35 USC § 103 (a) as being unpatentable over Farrell in view of Tsukikawa and Okada. In addition, the Examiner rejected claims 2, 3, 10, 12, and 18 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. These rejections have been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1 - 18.

2. Claims 2, 3, 10, 12, and 18 have been under 35 USC § 112, second paragraph. The applicant has amended these claims in accordance with the Examiner's rejection and therefore believes that these claims overcome this rejection.

3. Claims 1, 6, 9, 11, and 15 have been rejected under 35 USC § 102 (b) as being anticipated by Farrell et al. In particular, the Examiner references Figure 8 of Farrell as an apparatus that anticipates the present claims. The applicant disagrees with the Examiner's characterization of

the present invention in view of the art cited and states the following in support of his position.

Claim 1 of the present invention provides an edge sensitive detection circuit that accurately produces a latched logic value for an integrated circuit when that integrated circuit is in a state of transition (e.g., power down, reset, standby, and/or power up). As claimed, the edge sensitive detection circuit includes a filter module and a soft latch module. The filter module produces a pulse signal in response to an edge of an input logic signal and provides the pulse signal to the soft latch module. The soft latch module latches a logic value in accordance with the pulse signal.

Because the edge sensitive detection circuit of claim 1 does not require a clock signal to latch a logic signal, the software-hardware interdependency is overcome. As stated in the background section of the present patent application, the software-hardware interdependency results in one portion (e.g., software or hardware) needing the other to be functional before it can be functional in traditional triggering circuits.

With respect to claim 1, the clock synchronizing reset system 112, and its components, of Figure 8 of Farrell are a traditional triggering circuit. As taught, a reset signal is applied at least ten times to the input of the clock synchronizing reset system 112 (Column 21, lines 23 - 26). The edge sensitive detection circuit of claim 1 has no such ten-time limitation.

The reset conditioning circuitry 804 receives the reset signal and produces a conditioned reset signal therefrom. The conditioned reset signal must have a predetermined time duration before it is applied to the leading edge detector 808 (Column 21, lines 39 - 44). The edge sensitive detection circuit of claim 1 has no such time duration limitation.

The leading edge detector 808 includes a latch 824 that is clocked by clock input line 102, which supports an externally available clock signal (Column 21, lines 45 - 48). The clock input line 102 also clocks reset conditioning circuitry 804 (Column 21, lines 50 - 51). The edge sensitive detection circuit of claim 1 has no such clocking limitation.

The output of latch 824 is inverted and applied to gate 828, which also receives the conditioned reset signal of line 826. The output of gate 828 is thus representative of the leading edge of the reset signal of input line 802 and it is the output of the reset leading edge detector 808 (column 21, lines 51 - 56). The edge sensitive detection circuit of claim 1 includes no limitation regarding feed-forwarding of a conditioned reset signal to produce a leading edge of that signal.

As such, since the edge sensitive detection circuit of claim 1 does not include limitations with respect to: multiple inputting of a logic signal; time duration of a conditioned input signal; clocking of elements within the circuit; and feed-forwarding of the input signal, claim 1 is not anticipated by Farrell.

Claim 6 is dependent on claim 1, which has been shown to be allowable. Since claim 6 introduces additional patent subject matter, the applicant believes that claim 6 overcomes the present rejection.

Claim 9 claims an edge sensitive detection circuit that includes an input gating device, a processing module, a filter module, and a soft latch module. Since Farrell does not anticipate the filter module and the soft latch module, as discussed above with reference to claim 1, the applicant believes that claim 9 overcomes the present rejection.

Claims 11 and 15 are dependent on claim 9, which has been shown to be allowable. Since each of claims 11 and 15 introduces additional patent subject matter, the applicant believes that claims 11 and 15 overcome the present rejection.

4. Claims 2, 3, 7, 9, and 12 have been under 35 USC § 103 (a) as being unpatentable over Farrell in view of Tsukikawa (U.S. Patent No. 6,121,812). In particular, the Examiner states that Farrell discloses all the claimed invention except for having a latch element comprising specific components. Tsukikawa discloses in Figure 8 a latch circuit 30 that includes a first inverter 42 and a second inverting logic element (NAND gate 43). The applicant respectfully disagrees with the Examiner's characterization of the present invention in view of Farrell and Tsukikawa.

The applicant reasserts the arguments presented in the preceding section with respect to Farrell. Since Farrell does not teach or suggest an edge sensitive detection circuit as is presently claimed in claims 1 and 9, the dependent claims 2, 3, and 7 of claim 1 and claim 12 of claim 9 cannot be rendered cbvious by Farrell in view with any other art. In addition, the latch shown in figure 8 of Tsukikawa includes three logic elements NOR gate 41, inverter 42, and AND gate 43 and does not include an impedance. In contrast, the soft latch of the present claims includes two logic elements and an output impedance associated with the second logic element.

Therefore, the applicant believes that the present claims overcome the cited rejection of this section.

5. Claims 4, 5, 13, 14, 17, and 18 have been rejected under 35 USC § 103 (a) as being unpatentable over Farrell in view of Okada. In particular, the Examiner states that Farrell discloses all the claimed invention except for having a filter element comprising specific components. Okada discloses in Figure 3 an apparatus comprising a capacitor coupled to the input T1 and a gating circuit, including controlled impedance Q5, Q6, coupled to the capacitor such that the capacitor and an impedance of at least one element of the gating circuit are tuned based on the rise time and fall time of the input signal. The applicant respectfully disagrees with the Examiner's characterization of the present invention in view of Farrell and Tsukikawa.

The applicant reasserts the arguments presented in section 3 with respect to Farrell. Since Farrell does not teach or suggest an edge sensitive detection circuit as is presently claimed in claims 1, 9, and 17 the dependent claims 4 and 5 of claim 1, claims 13 and 14 of claim 9, and claim 187 of claim 17 cannot be rendered obvious by Farrell in view with any other art. In addition, the filter shown in figure 3 of Okada is substantially different than the filter module of the present invention. In particular, the filter of Okada includes a differential amplifier (Q2 and Q3) and a bias voltage source V_{BB}, and does not include an inverter. The filter of the present claims includes an inverter and does not include a differential amplifier or a bias voltage source.

Therefore, the applicant believes that the present claims overcome the cited rejection of this section.

6. Claim 8 has been rejected under 35 USC § 103 (a) as being unpatentable over Farrell in view of Tsukikawa and Okada.

The applicant asserts the arguments presented in the preceding sections to overccme the present rejection. Therefore, the applicant believes that the present claim overcomes the cited rejecticn of this section.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

2. (amended) The edge sensitive detection circuit of claim 1, wherein the soft latch mcdule comprises:

a first inverting logic element; and

a second inverting logic element having [a moderate impedance] an output impedance, wherein an input of the first inverting logic element is coupled to the [moderate] output impedance [output], wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the [moderate impedance] output impedance.

3. (amended) The edge sensitive detection circuit of claim 2, wherein the [first] second inverting logic element comprises an inverter and wherein the [second] first inverting logic element comprises at least one of an inverter and a NAND gate.

10. (amended) The edge sensitive detection circuit of claim 9 further comprises:

a second gating device that provides a second input logic signal to the processing module, [and wherein the filter module produces a second pulse signal in response to an edge of the processed logic signal] wherein the processing module produces a second prccessed logic signal based on the second input logic signal;

a second filter module operably coupled to receive the second processed logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second processed logic signal; and

a second soft latch module cperably coupled to receive the second pulse signal, wherein the second soft latch module latches a logic value in accordance with the second pulse signal.

12. (amended) The edge sensitive detection circuit of claim 9, wherein the soft latch mcdule comprises:

a first inverting logic element; and

a second inverting logic element having [a moderate impedance] an output impedance, wherein an input of the first inverting logic element is coupled to the [moderate] output impedance [output], wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the [moderate impedance] output impedance.

18. (amended) The edge sensitive detection circuit of claim 17, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having [a moderate impedance] an output impedance, wherein an input of the first inverting logic element is coupled to the [moderate] output impedance [output], wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the [moderate impedance] output impedance.

For the foregoing reascns, the applicant believes that claims 1 - 18 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

By: _____

Timothy W. Markison
Registration No. 33,534
Phone: (512) 342-0612
Fax No. (512) 342-1674

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